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DECLARATION

I, Peter Johnson, BA MITI, of Beacon House, Willow Walk, Woodley Park, Skelmersdale, Lancashire, WN8 6UR, hereby certify that to the best of my knowledge and belief the following is a true translation made by me, and for which I accept responsibility, of European patent application No 97460009.0

Signed this 16th day of June 1999

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The invention concerns an electrically modifiable multilevel non-volatile memory comprising autonomous refresh means. The invention more particularly finds an application in the field of memories with a large capacity, around several tens of megabits.

There are several techniques for increasing the density of memories. One of them consists of storing several information bits in the same memory cell. This is then referred to as multilevel memories. Conventional memories store one information bit per memory cell, that is to say two programming states. These states correspond to the presence or absence of electrical charges in the floating gate of the transistors making up the constituent memory cell. Multilevel memories, for their part, make it possible to store a larger number of programming states per memory cell.

The patent EP 0 340 107 describes an electrically modifiable non-volatile multilevel memory. Each cell in the memory is capable of storing n possible programming states, with n equal to at least three. These different programming states are obtained by varying the conduction threshold of the floating gate transistor making up the memory cell. In order to obtain this variation in conduction threshold, the cell is programmed more or less strongly by varying the intensity of the programming, that is to say either the voltage supplied to the cell or the duration of amplification of the voltage. For reading the information contained in the memory, a current or a voltage which is a function of the cell programming state is compared with n-1 main reference values in order to derive therefrom the programming state of the memory cell amongst n possible states.

However, the physical phenomena brought into play by the programming of such memory cells are not well controlled

industrially. As a result the currents issuing from the reference cells and the programmed cells are not known with great accuracy. They depend on many factors, including the reading voltage values applied to the cells. The current issuing from a program cell depends on the intensity of the programming, that is to say on the quantity of electrical charges injected into its floating gate. This quantity of charges depends on the programming voltage and the duration of application of this voltage, or even on the way in which it would be applied. There exists therefore a very great scatter between the current values of reference cells and cells programmed in a series of memories of the same manufacture.

It also happens that uncontrolled movements of electrical charges take place during operations of programming or erasing the memory. For example, during the programming of a memory cell of a multilevel memory of the FLASH EPROM type, a high voltage Vpp is applied to the word line connected to the control gate of the cell and a lower voltage Vp to the bit line connected to the drain of the cell. The sources of all the cells belonging to the same sector are connected to earth during programming. The cells connected to the same word line are then subjected to an electric field which may be responsible for a movement of electrical charges.

In addition, the programming state of a programmed memory cell degrades over time, that is to say the floating gate of the memory cells has a tendency to lose electrical charges over time. The retention of a memory cell lasts for around ten years. For high temperature conditions, this degradation is accelerated still further.

Finally, a large number of writing cycles applied to the cell can also impair the quality of the dielectric situated between the floating gate of the cell and the substrate. Thus a cell which has frequently been acted on may lose or gain electrical charges more easily than another cell.

All these variations are all the more of a problem since, in multilevel memories, the voltage or current ranges representing the different programming states are smaller because of their large number.

Faced with all these possible variations in the programming state of the cell, intermediate reference values are provided. These intermediate reference values define safety ranges which make it possible to predict any loss of a programming state. They are used for refreshing the memory cells. For this purpose, the reading current of a cell is compared with these intermediate reference values and in this way it is determined whether the cell should undergo supplementary programming.

It is therefore found that multilevel memories of the FLASH EPROM type, although they are non-volatile, need to be continually refreshed.

Normally, the operation of refreshing the memory or a sector of the memory is carried out under the control of a control unit external to the memory. Any access to the memory during the refresh operation is then impossible.

In addition, the refresh operation is generally triggered following a writing operation (programming or erasing) in the memory in order to remedy any disturbances which this type of operation might cause. This refresh mode does not take account of the phenomena of loss of electrical charges over time, in particular for memory cells which have frequently been acted on.

The aim of the invention is to remedy these drawbacks.

The object of the invention is an electrically modifiable non-volatile memory unit having a first matrix of non-volatile memory cells able to store at least two information bits, the said first matrix being divided into sectors, first means of

addressing and programming the said first matrix, first read and write circuits associated with the said first matrix, and a control circuit for controlling the whole, the said memory unit being characterised in that it also has refresh means under the control of the control circuit and a real-time clock delivering pulses for periodically triggering an operation of refreshing the memory cells of the said first matrix.

Thus the refresh operation in the memory unit of the invention is performed autonomously and requires no external command.

In addition, the refresh operation is carried out periodically in order to mitigate any phenomenon of gain or loss of electrical charges at the floating gate of the memory cells.

Preferably, the refresh operation takes place sector by sector.

According to a particular embodiment of the invention, the memory has a second matrix of static memory cells. The refresh operation is then performed in two steps:

- a step of duplicating, in the second matrix, information contained in a sector of the first matrix, and

- a step of refreshing the cells in the sector of the first matrix containing this information.

Thus the information in the cells in the course of being refreshed is accessible in read mode from the second matrix without interfering with the progress of the refresh step.

Other characteristics and advantages of the invention will emerge from a reading of the following detailed description which is given with reference to the accompanying drawings, in which:

- Figure 1 depicts an example embodiment of the memory according to the invention;

- Figure 2 depicts a flow diagram of an operation of refreshing the memory unit according to the invention, and

- Figure 3 depicts schematically a current curve generated in read mode by a memory cell as a function of its programming.

Figure 1 illustrates a preferred example of an embodiment of the memory unit according to the invention. By way of non-limitative example, the multilevel memory is of the FLASH EEPROM type.

The memory unit has a matrix 1 of non-volatile memory cells able to store several information bits. These memory cells are connected to a row decoder 3 and to a column decoder 4 itself associated with read and write circuits 5.

In the case of a memory of the FLASH EEPROM type, each cell consists of a floating gate transistor whose conduction threshold can be modified electrically by applying a suitable voltage to its electrodes. Thus, for this type of memory, a column programming voltage generator 6 is provided, supplying the drains by means of the read and write circuits 5 and supplying the sources by means of a source supply circuit 8. A row supply circuit 7 is also provided, for applying the programming voltage to the gates. These supply means receive a potential Vpp delivered by a so-called high-voltage generator (not shown).

In practice, a FLASH EEPROM memory is divided into sectors, which sectors each have a matrix of memory cells provided with a row decoder and a column decoder, associated read and write circuits and circuits supplying the rows and columns. For reasons of legibility, only one sector has been depicted in Figure 1.

The decoders 3 and 4 are connected to an address register 9. The read and write circuits 5 are connected to an input data register 10 and to an output data register 11. All the circuits 3 to 8 are controlled by the control circuit 2.

The control circuit 2 comprises refresh means 2A and is designed to interpret external control signals CD and internal control signals CORR and COMP. According to this interpretation, the control circuit supplies control signals CDa, CDd, CDi and RF. According to an advantageous embodiment, the internal control signals pass over an internal control bus.

The control circuit 2 is a programmed unit, for example of the programmable logic array (PLA) type, which controls all the circuits of the memory such as for example the supply circuits 6, 7 and 8. The role of the control circuit 2 is principally to control the operations of reading, programming and erasing the memory cells.

The memory unit communicates with the outside by means of an interface circuit (not shown) designed to receive read and write commands associated with address information, to receive the data to be written and to receive the read data.

The control circuit 2 sends control signals CDa CDd and CDi intended respectively for the address registers, the data registers and the other circuits in the memory unit. A refresh signal RF is also provided for indicating that a refresh operation is currently being carried out.

In order to implement the invention, the diagram of the memory unit is also supplemented with a certain number of circuits. First of all, a real-time clock 14 is associated with the control circuit 2. This clock can be backed up, for example, by a lithium battery integrated into the memory.

The real-time clock 14 periodically delivers clock pulses intended for the control circuit 2. Each pulse then triggers, at the control circuit 2, an operation of refreshing the memory cells of the matrix 1.

An address generator 2 associated with each sector of the matrix 1 is also provided for producing the addresses ADR of all the cells in the sector during the refresh operation. This generator is interposed between the address register 9 and the line 3 and column 4 decoders. When it is not acted on for refreshing the sector which is associated with it, the address register 12 directly transmits to the column and row decoders the address AD associated with an external command and, in this case, the address AD is equal to the address ADR.

In addition, an address comparator 13 is provided for comparing the external addresses AD and the addresses ADR generated by the address generator 12 during the refresh operations. This comparator makes it possible to determine whether the address associated with an external read or write command belongs to the sector of the matrix 1 currently being refreshed. A comparison signal COMP representing the result of the comparison is transmitted to the control circuit 2.

The control circuit 2 also receives a correction signal CORR sent by the read circuit and whose purpose is to trigger a supplementary programming of the cell currently being refreshed or an erasure of the sector followed by reprogramming. The address generator 12 and comparator 13 are activated by the refresh signal RF.

According to a preferred embodiment, a second matrix 15 of static memory cells is provided, organised in rows and columns so that the data of the sector currently being refreshed are accessible in read mode from the second matrix during the refresh step. Static memory cells are used since the time of a write cycle in the static cell is very short compared with

that of a dynamic cell or a redundant non-volatile cell. In addition, the rows of the second matrix are selected by means of a row decoder 16 whilst the columns are selected by a column decoder 17 associated with read and write circuits 18.

The refresh operation associated with this type of structure takes place in two steps: a step of duplicating, in the second matrix, the data of a sector of the first matrix, and a step of refreshing the cells of the duplicated sector of the first matrix.

The step of refreshing a sector takes place cell by cell. The correction signal CORR issuing from the read circuit associated with the read cell is designed to indicate to the control circuit 2 whether the cell needs to be corrected. The correction consists either of a supplementary programming of the cell, or of an erasure and then reprogramming of the sector associated with the cell.

The decoders of rows 16 and columns 17 receive an address supplied by a conversion circuit 19. The purpose of the conversion circuit is to transform the address ADR into an address adapted to the matrix 15. This is because the size of the matrix 15 is equal to the size of a sector of the matrix 11. The new address issuing from the conversion circuit therefore has no sector indication. For example, the conversion circuit eliminates the bits of the address ADR indicating a matrix sector, in general the most significant bits.

The read and write circuits 18 are connected with an input data register 20 and an output data register 21. The input data register 20 is connected with the output data register 11 for duplicating data of the sector to be refreshed. In addition, a multiplexer 20 receives the data coming from the two output registers 11 and 21, and selects the data to be supplied at the output of the memory. The output of an AND

gate 23 is connected to the selection input of the multiplexer 20. The signals COMP and RF are applied to the inputs of the AND gate 23. Thus the data delivered by the memory unit following an external read command come from the matrix of static cells if the sector concerned is the sector currently being refreshed.

Apart from the refresh operations, the operations of reading and writing in the matrix 1 are performed in the same way as for a conventional non-volatile memory under the control of the control circuit 2.

Figure 2 depicts a flow diagram of a refresh operation adapted to the memory unit of Figure 1. Following a clock signal delivered by the real-time clock 14, the control circuit 2 triggers a refresh operation. A first sector of the matrix 1 is selected. In a first step, the data of the selected sector are duplicated in the second matrix 15. The circuits to which the current refresh operation does not relate are accessible in read and write mode using external commands.

The duplication step is followed by a refresh step in which the cells of the selected sector are read one after the other. To do this, the address generator 12 of the sector currently being refreshed supplies addresses to the row decoder 3 and to the column decoder 4. In order to determine the programming state of the cell read, the current issuing from the cell subjected to the read voltage is compared with principal reference levels. This current is also compared with intermediate reference levels in order to determine whether the read cell should undergo supplementary programming or be erased and then reprogrammed.

Figure 3 depicts schematically a current curve generated in read mode by a memory cell as a function of its programming. This figure illustrates the case of a memory unit where the cells are capable of storing four programming states, that is

to say two information bits. The principal reference values IR1, IR2 and IR3 are current levels for defining four programming states. The state 11 corresponds to a cell which, in read mode, generates a current higher than the level IR1. The state 10 corresponds to the cell which, in read mode, generates a current lying between the level IR1 and the level IR2. The state 01 corresponds to a cell which, in read mode, generates a current lying between the level IR2 and the level IR3. Finally, the state 00 corresponds to a cell which, in read mode, generates a current lower than the level IR3.

Intermediate reference levels are also defined by current levels IR0B, IR1A, IR1B, IR2A, IR2B and IR3A.

These intermediate reference levels define safety ranges. In this type of memory, it is considered that a cell which is to be programmed to the n^{th} state (the state 11 is the first state) must not only supply a current lying between IRn-1 and IRn but more precisely supply a current lying between IRn-1A and IRn-1B. If the cell reading current is in between IRn-1 and IRn-1A, it is considered that the cell is insufficiently programmed and the cell must undergo supplementary programming. Conversely, if the cell reading current is between IRn-1B and IRn, the cell must be erased. The erasure taking place in a global fashion in a memory of the FLASH type, the entire sector containing the cell is to be erased; the sector will then be reprogrammed.

If reference is made once again to Figure 2, each cell in the matrix is thus read so as to determine whether it requires to undergo reprogramming for erasure followed by reprogramming. These reprogramming or erasure commands are transmitted to the control circuit 2 by means of the correction signal CORR.

Where the cell is insufficiently programmed, it undergoes supplementary programming, for example in the form of a voltage pulse applied to the gate of the memory cell. The

following cell is next passed to.

Where the cell requires erasure, the sector associated with the cell is erased and is reprogrammed entirely. The following sector is next passed to directly.

All the cells in the matrix 1 are thus checked. At the end of each elementary refresh step, the address generator is incremented.

In addition, an autonomous supply device (not shown) is provided for supplying the memory unit so that the refresh operation is performed normally when the device including the memory unit is not powered. It could be envisaged activating the autonomous supply device at each pulse of the clock 14 for a certain period in the absence of a supply provided by the system.

As seen previously, the data of the matrix 1 remain accessible in read mode during the refresh operation. This is because, if it is adapted to read a data item belonging to a sector different from the sector currently being refreshed, the reading takes place in a conventional fashion without interrupting the refresh operation. On the other hand, if it is attempted to read a data item stored in a sector currently being refreshed, there are two possible cases. If the duplication of the sector of the matrix 1 has ended, the corresponding data item in the matrix 1 is read, otherwise the duplication is interrupted and the data item is read in the matrix 1.

Moreover, any writing operation (programming or erasure) triggered by an external command on a sector of the matrix 1 may modify the operation of refreshing the matrix. If the address associated with the write command points to a sector of the matrix 1 currently being refreshed, the refresh operation is interrupted in order to allow the writing

operation to take place. The refresh operation then resumes at the following sector.

It can be envisaged inserting the refresh means of the invention in conventional memories.

Otherwise, if the write operation concerns a sector other than the one currently being refreshed, it takes place in a conventional fashion without interrupting the refresh operation.

According to a preferred embodiment, the refresh operation takes place every hour.

CLAIMS

1. Electrically modifiable non-volatile memory unit having a first matrix (1) of non-volatile memory cells able to store at least two information bits, the said first matrix being divided into sectors, first means of addressing (3, 4) and programming (6, 7, 8) the said first matrix, first read and write circuits (5) associated with the said first matrix (1), and a control circuit (2) for controlling the assembly, the said memory unit being characterised in that it also has refresh means (2A) under the control of the control circuit (2) and a real-time clock (14) delivering pulses for periodically triggering an operation of refreshing the memory cells of the said first matrix (1).

2. Memory unit according to Claim 1, characterised in that the operation of refreshing the first matrix (1) is performed sector by sector.

3. Memory unit according to one of Claims 1 or 2, characterised in that it has a second matrix (15) of static memory cells, second means of addressing (16, 17) the said second matrix (15), the refresh operation being performed in two steps: a step of duplicating, in the second matrix (15), information contained in the first matrix (1), and a step of refreshing the memory cells of the first matrix (1) containing this set of information, so that, during the refresh step, the information in the cells in the course of being refreshed is accessible in read mode from the second matrix (15).

4. Memory unit according to one of Claims 2 or 3, characterised in that the capacity of the second matrix (15) is equal to the capacity of a sector of the first matrix (1).

5. Memory unit according to any one of Claims 1 to 4, characterised in that a refresh operation is triggered every hour.

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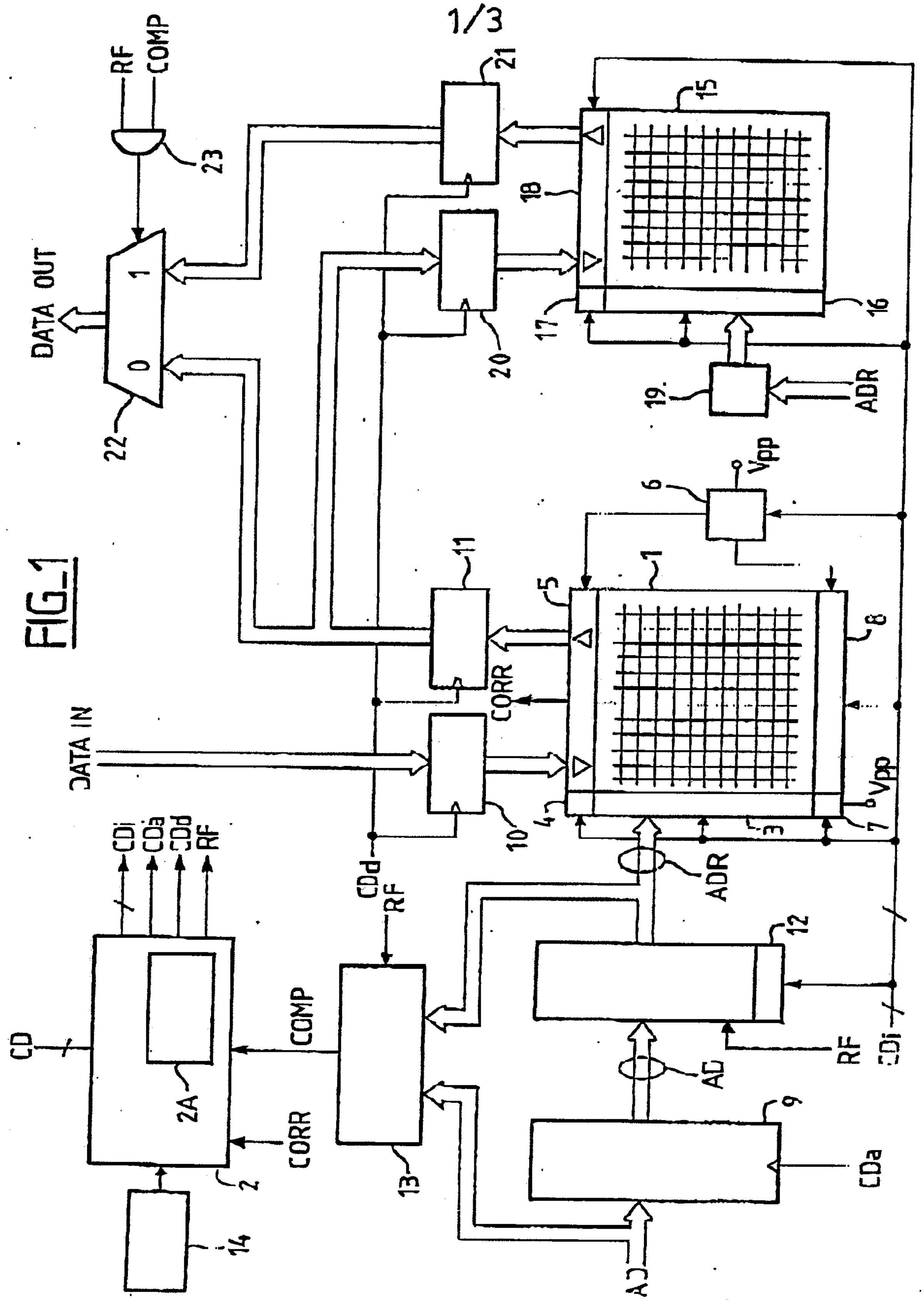
DATA OUT
RF
COMP
23
22
21
20
15
18
17
16
19
ADR
6
Vpp
11
5
1
8
DATA IN
CORR
10
4
3
7
Vpp
CDd
RF
ADR
12
CDi
CDa
CD
2A
COMP
CORR
2
14
13
AD
9
CDa
RF
CDi

FIG_1

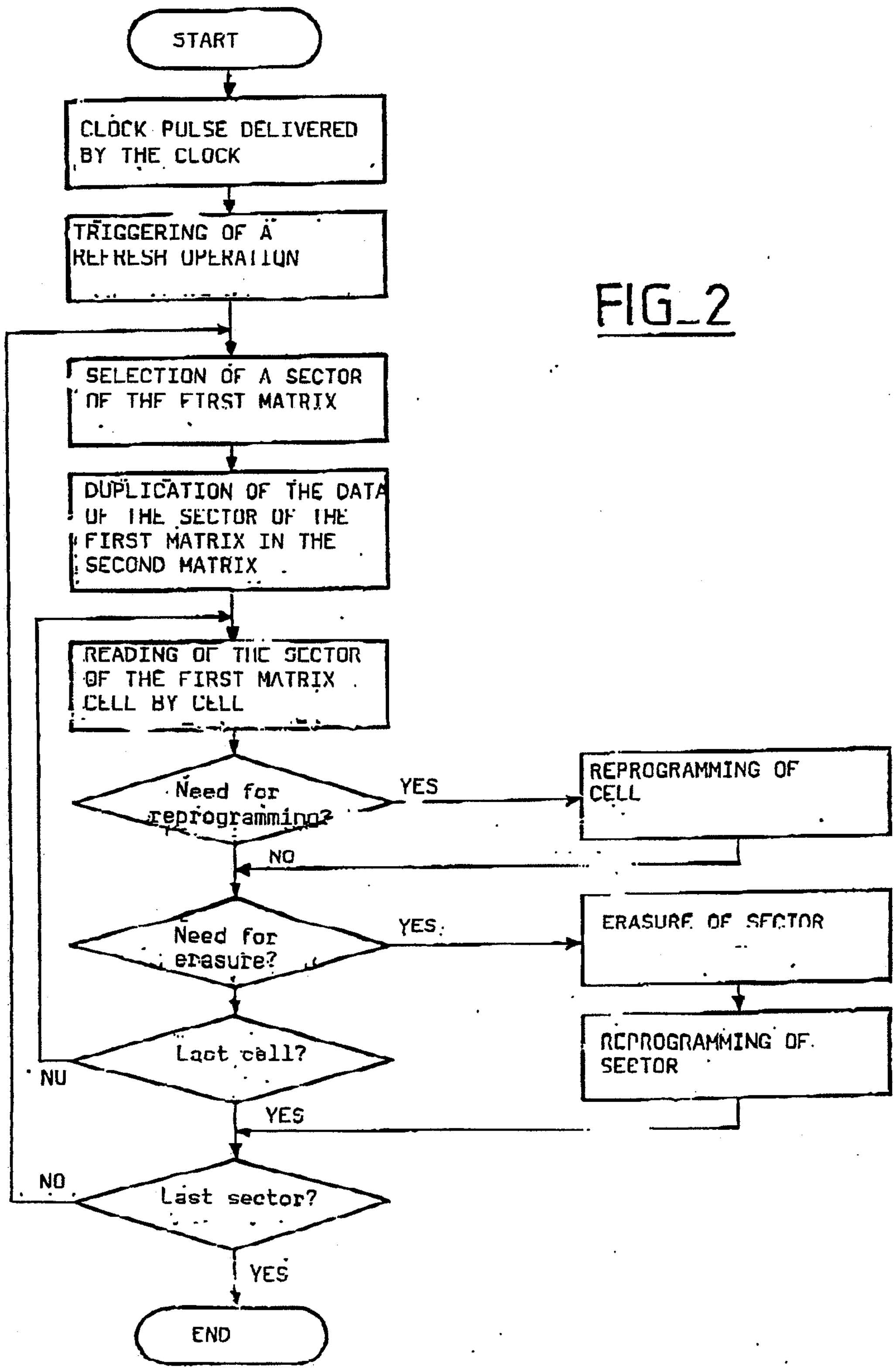
START
CLOCK PULSE DELIVERED BY THE CLOCK
TRIGGERING OF A REFRESH OPERATION
SELECTION OF A SECTOR OF THE FIRST MATRIX
DUPLICATION OF THE DATA OF THE SECTOR OF THE FIRST MATRIX IN THE SECOND MATRIX
READING OF THE SECTOR OF THE FIRST MATRIX CELL BY CELL
Need for reprogramming?
YES
REPROGRAMMING OF CELL
NO
Need for erasure?
YES
ERASURE OF SECTOR
REPROGRAMMING OF SECTOR
Last cell?
NO
YES
Last sector?
NO
YES
END

FIG_2

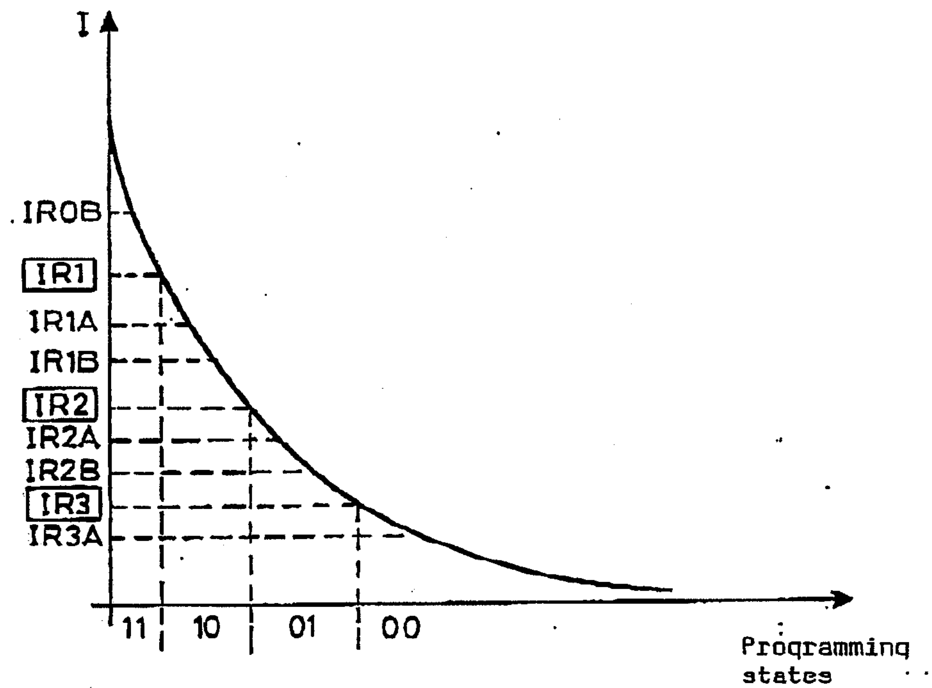
I
IR0B
IR1
IR1A
IR1B
IR2
IR2A
IR2B
IR3
IR3A
11
10
01
00
Programming states

FIG_3